PATENT APPLICATION
Q46364

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yoshinori MATSUI

Reissue Application of U.S. Patent
No. 5,444,305 issued on August 22, 1995

Filed: Herewith

For: SEMICONDUCTOR MEMORY CIRCUIT

REISSUE DECLARATION UNDER 37 C.F.R. § 1.175

I, Yoshinori Matsui, of Tokyo, Japan, do hereby declare and state as follows:

My residence, post office address, and citizenship are as stated below next to my name.

I believe that I am the original, first, and sole inventor of the invention "SEMICONDUCTOR MEMORY CIRCUIT" which is described and claimed in the above-identified U.S. Patent No. 5,444,305, issued August 22, 1995 and assigned to NEC Corporation, the specification of which is submitted with this application for reissue; and that I have reviewed and understand the contents of the specification, including the claims, as amended in this application for reissue.

In compliance with 37 C.F.R. § 1.175(a)(7), I hereby acknowledge my duty to disclose information of which I am aware which is material to the examination of this application for reissue.

I hereby claim foreign priority benefits under 35 U.S.C. §§ 119 or 365 from the following foreign application for patent: Japanese Patent Application No. 4-172229, filed in Japan on June 30, 1992. The priority document was filed in U.S. patent application 08/084,017.

Further, in compliance with 37 C.F.R. §§ 1.175(a)(1)-(a)(3), I hereby declare and state that the above-identified U.S. Patent No. 5,444,305 is believed to be at least partly inoperative for the reason that I claimed less than I had the right to claim in the patent.

The purpose of seeking a reissue patent is to address the insufficiency in the patented claims by presenting new claims which are commensurate with the true scope of my invention.

Pursuant to 37 C.F.R. § 1.175(a)(5)-(6), I below describe the particular errors in the patent, how these errors occurred, and I hereby aver that such errors arose without any deceptive intention.

REISSUE DECLARATION UNDER 37 C.F.R. § 1.175
REISSUE APPLICATION OF U.S. PATENT NO. 5,444,305

A. Errors in the patent

The specific errors in the patent, i.e., every difference between the original patent and the claims sought to be added by this reissue application, are identified below.

The subject matter encompassed by original patent claims 1-3 is literally too narrow in certain respects to afford patent coverage commensurate with the true scope of my invention. As well, the patent lacks any dependent claims and fails to comprehensively claim the invention.

In general, claim 1 recites entirely too many specific limitations even to approximate the proper scope of my invention which resides not merely in the arrangement of the myriad particular circuits but more correctly in the overall arrangement of the memory cell blocks and the amplifier blocks. Claim 2 includes an unnecessary limitation in that it recites input-output circuits not necessary for patentability. Claim 3, like claim 2, also recites input-output circuits which are unnecessary for patentability.

New claims 4-20 presented in this reissue application include independent claims 4, 12, and 19. These new independent claims do not include all of the specific structure of issued claim 1, and are free of the input-output circuits of issued claims 2 and 3. Such limitations which are unnecessary for patentability are included in the claims which depend from new independent claims 4, 12, and 19. Therefore, these new claims more properly claim the true scope of my invention, and thus remedy the basic error in claiming less than I had a right to claim.

More particularly, new independent claim 4 provides a claim in the patent which does not have the above-identified error of claim 2; new independent claim 12 provides in the patent a claim which corrects the error of claim 3 being too narrow; and new independent claim 19 provides in the patent a claim that is even broader in some respects than new independent claims 4 and 12, thus claiming the invention with the scope to which it is entitled.

The specific differences between new claims 4-20 and the original patent claims, and the reasons for these differences, are explained below.

Claims 4-12

New independent claim 4 corrects an error in issued claim 2. Claim 2 has an error in that it has too narrow of a scope. In addition, claim 2 has an error in that it lacks the dependent claims necessary so as comprehensively to claim the subject matter of the invention.

Claim 2 has a scope that is too narrow because it includes limitations unnecessary to patentability, to wit, first and second input-output circuits. The first and second input-output circuits are believed to be unnecessary to the patentability of the claim because the subject matter of the claim could have been patentably distinguished with reference only to its simplified layout of a memory circuit with a particular arrangement of memory cell blocks, amplifier blocks, and data lines. I now explain how new claim 4 corrects this error.

New independent claim 4 recites exactly the same semiconductor memory device as set forth in issued claim 2 with two exceptions. The first exception is that claim 4 does not include the following requirement (which is included in lines 20-22 of claim 2, as shown in the Reissue Application which is being filed concurrently herewith): ", said first and second amplifier blocks thereby being coupled to a common first input-output circuit via said first data line independently from said third amplifier block". The second exception is that claim 4 does not include the following requirement (which is included in lines 24-25 of claim 2): "and thereby coupling said third amplifier block to a second input-output circuit independently from said first and second amplifier blocks".

Since new claim 4 omits the first and second input-output circuits, which are not necessary for patentability, claim 4 corrects the above-identified error of issued claim 2.

New dependent claims 5-11 correct the other error of claim 2, namely, that claim 2 as issued lacks the dependent claims necessary to comprehensively claim the invention. New dependent claims 5-11 add requirements to the subject matter of claim 4 as described now with particularity.

New dependent claim 5 (i.e., 5/4) contains limitations substantially similar to those which were omitted from claim 4 but included in issued claim 2. The limitations contained in claim 5, however, are not identical to those which were omitted from claim 4 but included in issued claim 2. In particular, claim 5 requires first and second interface circuits instead of "input-output" circuits as required in issued claim 2. I respectfully submit that the recitation of interface circuits encompasses more kinds of circuits than the narrower recitation of input-output circuits.

New claim 6 (i.e., 6/5/4) adds limitations not included in issued claim 2, to wit, the requirement for the first and second interface circuits to receive read data from the memory cell blocks.

New claim 7 (i.e., 7/6/5/4) also adds limitations not included in issued claim 2. Claim 7 requires that the first and second interface circuits transfer write data for the memory device.

New claim 8 (i.e., 8/4) adds limitations not included in issued claim 2. In particular, claim 8 requires that the memory cells of the memory cell blocks be arranged in rows and columns to form a matrix. Moreover, claim 8 adds the new requirement that the first group of memory cells be in either an even or an odd numbered column, and that the second group be in the other (i.e., if the first group is even, the second group is odd).

New claim 9 (i.e., 9/8/4) adds further limitations not included in issued claim 2. To be precise, claim 9 substantially describes a folded bit line structure. Also, new claim 9 describes how the third amplifier block is connected to the bit lines of its adjacent memory cell blocks.

New claim 10 (i.e., 10/9/8/4) adds limitations relating to first transfer gates, which were not mentioned in issued claim 2.

New claim 11 (i.e., 11/10/9/8/4) requires second transfer gates, another requirement not included in issued claim 2.

Claims 12-18

New independent claim 12 corrects an error in issued claim 3. Claim 3 has an error in that it has too narrow of a scope. Claim 3 has an additional error in that it lacks the dependent claims necessary so as comprehensively to claim the full extent of the invention.

Like issued claim 2, claim 3 has a scope that is too narrow because it includes limitations unnecessary to patentability, to wit, first and second input-output circuits. The first and second input-output circuits are believed to be unnecessary to the patentability of the claim because the subject matter of claim 3 could have been patentably distinguished with reference only to its simplified layout of a memory circuit with a particular arrangement of memory cell blocks, amplifier blocks, and data lines. I now explain how new claim 12 corrects this error.

New independent claim 12 is very similar to claim 3 in a substantive manner, but differs in that the claim omits any mention of the input-output circuits. Since new claim 12 omits the first and second input-output circuits, which are not necessary for patentability, claim 12 corrects the above-identified error of issued claim 3.

New dependent claims 13-18 correct the above-identified additional error of issued claim 3. That is, new dependent claims 13-18 (each of which depends directly or indirectly from new independent claim 12) provide the additional limitations necessary for the comprehensive claiming of the full extent of the invention.

In particular, new claim 13 (i.e., 13/12) requires data transfer circuits. The requirement for input-output circuits was omitted from independent claim 12 to correct an error in issued claim 3 and was moved to this dependent claim. Instead of reciting "input-output circuits", however, new claim 13 requires data transfer circuits.

New claim 14 (i.e., 14/13/12) adds a limitation not included in issued claim 3. That is, new claim 14 requires that the data transfer circuits handle read data of the memory device via first and second data lines.

New claim 15 (i.e., 15/12) includes the requirement that the memory cells be arranged in rows and columns with particular limitations relating to even and odd numbered columns. These requirements were not included in issued claim 3.

New claim 16 (i.e., 16/15/12) adds the requirement for a folded bit line structure and particular limitations relating to the coupling between amplifier blocks and their adjacent memory cell blocks. These requirements were not included in issued claim 3.

New claim 17 (i.e., 17/16/15/12) adds limitations not included in issued claim 3. In particular, claim 17 requires first and second transfer gate transistors which were not mentioned in claim 3.

New claim 18 (i.e., 18/17/16/15/12) adds the requirement for a switching circuit responsive to a selection signal; this requirement was not included in issued claim 3.

Claims 19 and 20

The patent is inoperative in that issued claims fail to recite the scope to which the invention is entitled. New independent claim 19 is even broader, in some respects, than any of independent claims 1, 2, 3, 4, and 12. By adding new independent claim 19, I achieve patent protection of a scope having the breadth to which the invention is entitled.

New claim 19 requires "first to N-th" amplifier blocks, instead of the plurality of amplifier blocks mentioned in claims 2, 3, 4, and 12, and instead of the plurality of

selection/sense amplifier circuits mentioned in claim 1. Similarly, new claim 19 requires "first to (N-1)-th memory cell blocks", instead of the plurality of memory cell blocks required in claims 2, 3, 4, and 12, and instead of the plurality of memory cell arrays required in claim 1.

In new claim 19, the first data line is "coupled" to "said first amplifier block and said N-th amplifier block", whereas in the other claims the first data line is coupled to the amplifier blocks on the ends of the array and also is isolated from another component. New claim 19 does not require the isolation of the first data line.

Claim 19 is thus not as narrow as the other independent claims in that it does not require the isolation of the first data line. Claim 19 is believed to more correctly claim the full breadth of patent protection to which my invention is entitled.

New dependent claim 20 (i.e., 20/19) adds to the invention as claimed in claim 19 the requirements for a signal line in each amplifier block, and describes a particular coupling for the signal lines for the first and for the (N-1)-th amplifier blocks.

B. How the above errors arose or occurred

Having discussed above the particular errors in the patent for which correction by reissue is sought, and having pointed out every difference between the original claim and reissue claim pursuant to 37 C.F.R. § 1.175(a)(3), I now explain how the errors arose or occurred, as required by 37 C.F.R. § 1.175(a)(5).

The errors arose during preparation and prosecution of U.S. Application No. 08/084,017 (the '017 application) which issued as U.S. Patent No. 5,444,305 (the '305 patent). Through oversight, I failed initially to have included claims having the scope of new claims 4-20, which are of varying scope and which are broader in at least some respects and narrower in other respects than original patent claims 1-3.

Through the Intellectual Property Division (IPD) of my company, NEC Corporation, I provided a substantially complete draft application to my U.S. attorneys (the Sughrue law firm), shortly before the expiration of the one year period for claiming foreign priority from my Japanese parent application and, after review, my U.S. attorneys filed the application in the U.S. Patent and Trademark Office.

In preparing the draft patent application, IPD failed to include claims having scopes such as that of the new claims proposed herewith.

The error of not including claims such as new claims 4-20 was not discovered during prosecution of the '017 application. In particular, the Examiner allowed dependent application claim 3 in the first Office Action. The IPD drafted an Amendment in which this claim was placed in independent form (this amended claim issued as claim 1). Two new claims 4 and 5 (which issued as claims 2 and 3, respectively) were added as well. These two new claims were directed to the invention in a different scope, but still were insufficient with respect to what I had a right to claim. This draft Amendment was sent to my U.S. attorneys shortly before the time limit for responding to the Office Action. The U.S. attorneys also failed to appreciate the full breadth of that to which I had a right to claim.

In the second Office Action, application claims 3 and 4 were rejected under only 35 U.S.C. § 112, second paragraph. IPD handled the rejection without a particular review of the scope of each claim. The '305 patent was thus passed to issue.

My company recently has reviewed the '305 patent in connection with the ordinary course of its business. During this review, the IPD asked me to review the '305 patent. I indicated to my company the importance of the '305 patent from a technical standpoint, and the IPD and I reviewed the claims to detect any possible insufficiency.

This review revealed that an error exists in the claims because they are not directed to the full scope of the invention (as already explained above, in detail).

New claims 4-20 are therefore being added by this reissue application in order to correct a deficiency in the patent, *viz.*, that through an oversight I failed to include claims having a scope commensurate with my true invention. New claims 4-20 particularly point out and distinctly claim my invention, and are believed to be patentable over the prior art.

I hereby appoint John H. Mion, Reg. No. 18,879; Donald E. Zinn, Reg. No. 19,046; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Robert G. McMorrow, Reg. No. 19,093; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I.

REISSUE DECLARATION UNDER 37 C.F.R. § 1.175
REISSUE APPLICATION OF U.S. PATENT NO. 5,444,305

Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484, Mark Boland, Reg. No. 32,197, William H. Mandir, Reg. No. 32,156, Scott M. Daniels, Reg. No. 32,562, Brian W. Hannon, Reg. No. 32,778 and Abraham J. Rosner, Reg. No. 33,276; Bruce E. Kramer, Reg. No. 33,725; Paul F. Neils, Reg. No. 33,102; and Brett S. Sylvester, Reg. No. 32,765, my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and request that all correspondence about the application be addressed to **SUGHRUE, MION, ZINN, MACPEAK & SEAS,** PLLC, 2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3202.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: August 18, 1997

Inventor: Yoshinori Matsui
First Name Last Name

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PATENT APPLICATION
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In re the Application of

Yoshinori MATSUI

Reissue Application of U.S. Patent
No. 5,444,305 issued on August 22, 1995

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ASSENT OF ASSIGNEE TO REISSUE

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

NEC Corporation, the Assignee of the entire right, title, and interest of the invention described and claimed in the above-identified U.S. Patent No. 5,444,305, hereby assents to the reissue of said patent in accordance with the Reissue Declaration and accompanying papers submitted herewith.

NEC Corporation

Date: August 19, 1997

Signature

Shigemichi Nidaira
Typed or printed name

Vice President
Intellectual property
Title

Assignment

Appln. No. 08/084,017
Filed June 30, 1993

Whereas, I/We, YOSHINORI MATSUI
Tokyo, Japan
of

hereinafter called assignor(s), have invented certain improvements in

SEMICONDUCTOR MEMORY CIRCUIT

and executed an application for Letters Patent of the United States of America therefor on June 29, 1993 ; and

Whereas, NEC Corporation
7-1, Shiba 5-chome, Minato-ku,
Tokyo, Japan

(assignee), desires to acquire the entire right, title, and interest in the application and invention, and to any United States patents to be obtained therefor;

Now therefore, for valuable consideration, receipt where of is hereby acknowledged,

I/We the above named assignor(s), hereby sell, assign and transfer to the above named assignee, its successors and assigns, the entire right, title and interest in the application and the invention disclosed therein for the United States of America, including the right to claim priority under 35 U.S. Code 119, and I/We request the Commissioner of Patents to issue any Letters Patent granted upon the invention set forth in the application to the assignee, its successors and assigns; and I/We will execute without further consideration all papers deemed necessary by the assignee in connection with the United States application when called upon to do so by the assignee.

Signed at Tokyo, Japan on June 29, 1993

Yoshinori Matsui
YOSHINORI MATSUI

Witness Date

Hirinori Takahashi June 29, 1993

Mutsuya Asano June 29, 1993

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